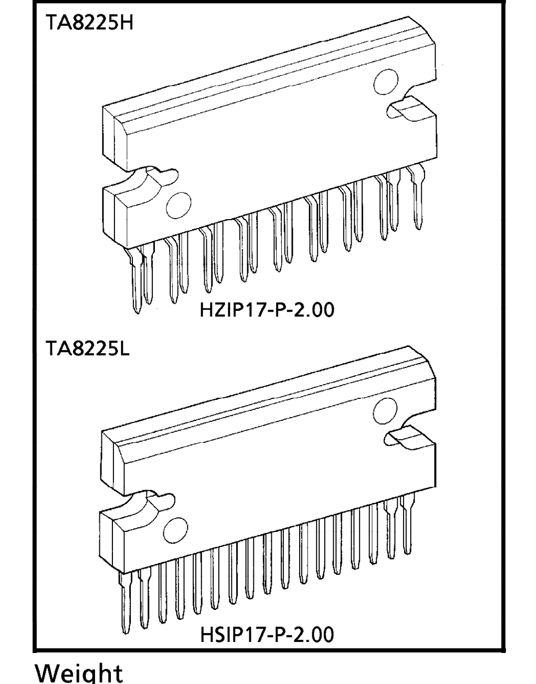
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8225H, TA8225L

45W BTL AUDIO AMPLIFIER

The TA8225H, TA8225L is BTL audio power amplifier for consumer application.
It is designed for high power, low distortion and low noise.
It contains various kind of protectors and the function of stand-by SW.
In addition, the functions of output short or over voltage detection and junction temperature are involved.



Weight
HZIP17-P-2.00 : 9.8g (Typ.)
HSIP17-P-2.00 : 9.8g (Typ.)

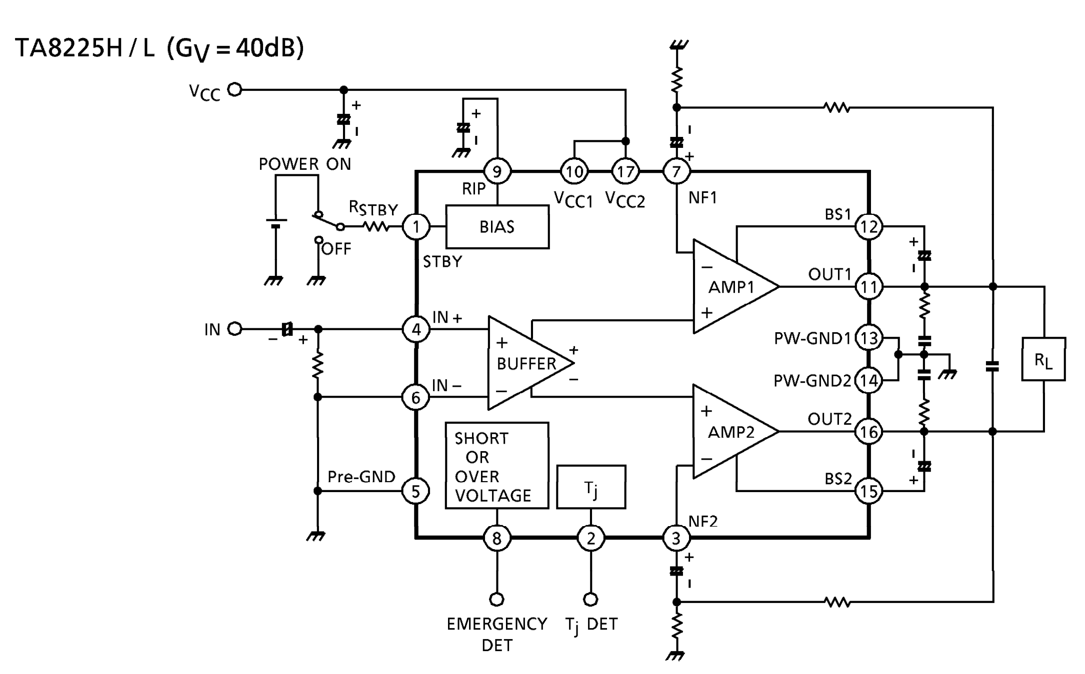
FEATURES

- High Power
  : $P_{OUT\,(1)} = 45W$ (Typ.)
  ($V_{CC} = 14.4V$, $f = 1kHz$, $THD = 10\%$, $R_L = 2\Omega$)
  : $P_{OUT\,(2)} = 40W$ (Typ.)
  ($V_{CC} = 13.2V$, $f = 1kHz$, $THD = 10\%$, $R_L = 2\Omega$)
  : $P_{OUT\,(3)} = 24W$ (Typ.)
  ($V_{CC} = 13.2V$, $f = 1kHz$, $THD = 10\%$, $R_L = 4\Omega$)
- Low Thermal Resistance
  : $\theta_{j-c} = 1.5°C/W$ (Infinite Heat Sink)
- Excellent Output Power Band Width
  : $P_{OUT\,(4)} = 18W$ (Typ.)
  ($V_{CC} = 13.2V$, $f = 50Hz \sim 20kHz$, $THD = 1\%$, $R_L = 4\Omega$)
- Low Distortion Ratio
  : $THD = 0.015\%$ (Typ.) Z
  ($V_{CC} = 13.2V$, $f = 1kHz$, $P_{OUT} = 4W$, $R_L = 4\Omega$)
- Built-in Stand-by Function (With pin ① set at high, power is turned ON)
- Built-in Output Short or Over Voltage Detection Circuit, Output to V_{CC} and Output to GND Short.
  (Pin ⑧ : Open Collector)
- Built-in Junction Temperature Detection Circuit. (Pin ② : Open Collector)
- Built-in Various Protection Circuits
  - Thermal Shut Down, Over Voltage
  - Output to GND Short
  - Output to V_{CC} Short
  - Output to Output Short
- Operating Supply Voltage : $V_{CC\,(opr)} = 9 \sim 18V$

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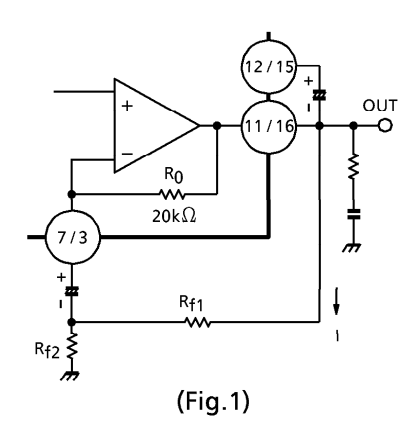
BLOCK DIAGRAM

TA8225H / L ($G_V = 40dB$)



CAUTION FOR USE AND METHOD OF APPLICATION

1. Voltage gain adjustment



(Fig.1)

Voltage gain G_V of this IC is decided by the external feedback resistors R_{f1} and R_{f2}.
Gain fluctuation by temperature can be made smaller than they are housed in IC.
Voltage gain G_V is decided by the following expression :

If $R_0 = 20k\Omega \gg R_{f1} > R_{f2}$ $\quad G_V \fallingdotseq 20\log \frac{R_{f1} + R_{f2}}{R_{f2}} + 6 \text{ (dB)}$

If $R_0 = 20k\Omega > R_{f1} > R_{f2}$ $\quad G_V \fallingdotseq 20\log \frac{(R_0 // R_{f1}) + R_{f2}}{R_{f2}} + 6 \text{ (dB)}$

If R_{f1} and R_{f2} are made small, the following problems may be caused :

(1) When output short is released, output DC voltage is not restored.
(2) Fluctuation of output DC voltage by current I in (Fig.1).

If voltage gain is made small excessively, oscillation may be taken place and therefore, this IC shall be used at $G_V = 34dB$ or above.

2. Preventive measure against oscillation

For preventing the oscillation, it is advisable to use C_4, the condenser of polyester film having small characteristic fluctuation of the temperature and the frequency.
the condenser (C_6) between input and GND is effective for preventing oscillation which is generated with feedback signal from an output stage.
The resistance R to be series applied to C_4 is effective for phase correction of high frequency, and improves the oscillation allowance.
Since the oscillation allowance is varied according to the causes described below, perform the temperature test to check the oscillation allowance.

(1) Voltage gain to be used (G_V Setting)
(2) Capacity value of condenser
(3) Kind of condenser
(4) Layout of printed board

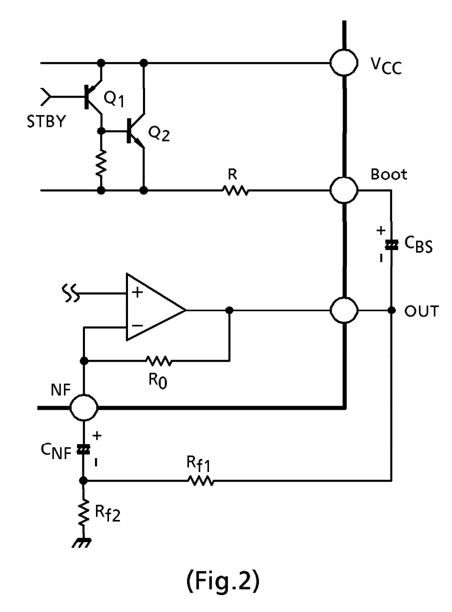
In case of its use with the voltage gain G_V reduced or with the feedback amount increased, care must be taken because the phase-inversion is caused by the high frequency resulting in making the oscillation liable generated.

3. Pop noise

A pop noise generated when the power source is turned ON depends on rise times of the in-phase side output (⑪pin) and the negative-phase side output (⑯pin), that is, output offset voltage.
The following two points may be pointed out as causes for generation the output offset voltage :

(1) In-phase and negative-phase NF capacitor charging times
(2) Input offset voltage

Especially, the factor (2) relates to the pop noise level.



(Fig.2)

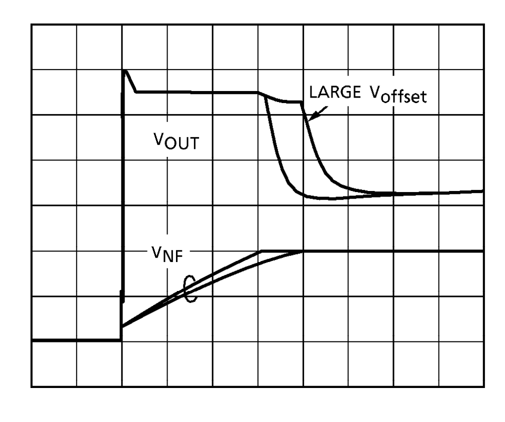
(1) In-phase and negative phase NF capacitor charging time

In (Fig.2), when the power source is turned ON, Q_1 and Q_2 are turned ON, and NF capacitors are charged in the route of V_{CC}→Q_2→R→Boot→C_{BS}→OUT→R_0→C_{NF}. For instance, if the capacity of an in-phase capacitor is not properly paired with that a negative-phase capacitor, output offset voltage = pop noise is produced because a charging time of NF capacitor differs between the in-phase and negative-phase outputs.

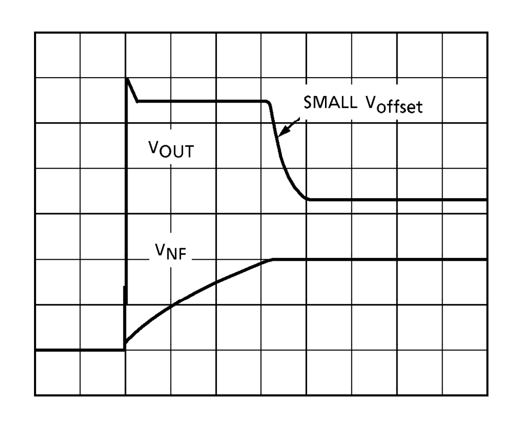
Therefore, to suppress the pop noise it is necessary to properly pair the in-phase and negative-phase NF capacitors. Output and NF DC voltage waveforms by the pairing of NF capacitors : C_{NF} are shown in (Fig.3) and (Fig.4).

Further, voltage waveforms are shown when the power source was turned ON, under the following conditions :

V_{CC} = 13.2V, R_L = 4Ω, Ta = 25°C, and input shot-circuit.
Output DC Voltage V_{OUT} : (2V / div, 200ms / div)
NF DC Voltage V_{NF} : (1V / div, 200ms / div)



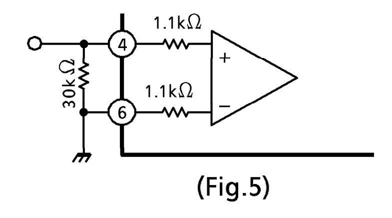
LARGE V_{offset}
(When C_{NF} are improperly paired)
(Fig.3)



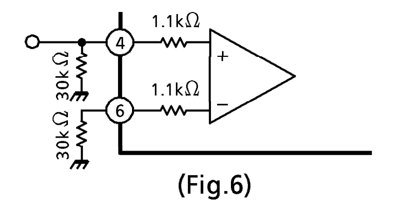
SMALL V_{offset}
(When C_{NF} are properly paired)
(Fig.4)

(2) Input offset voltage

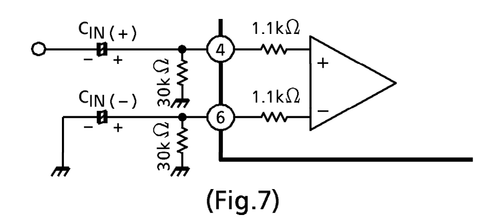
Input offset voltage is increased by as many times as a gain and appears as output offset voltage.
Input offset voltage is affected by an external resistor in addition to properness of pair of capacitor in IC.
An example of a general application circuit is shown in (Fig.5). In this case, input to the differential amplifier composing the buffer amplifier is decided to be 30kΩ + 1.1kΩ = 31.1kΩ at the IN (+) side and 1.1k at the IN (−) side. Therefore a rising difference of about 30 times between the IN (+) side and the IN (−) side.
So, to fit input offset voltages, it is possible to suppress the input offset voltage by adjusting it to 31.1kΩ both at the IN (+) and IN (−) sides according to the application example shown in (Fig.6). As input coupling capacitors are used in actual set, the circuit shown in (Fig.7) is considered. In this case, it is necessary to take the utmost care of proper pair of $C_{IN(+)}$ and $C_{IN(-)}$.



(Fig.5)



(Fig.6)



(Fig.7)

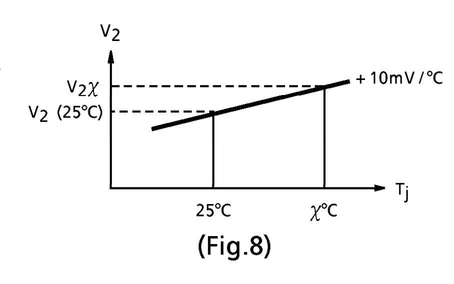
Pop noise level affected by input offset voltage shall be checked on an actually mounted set.

4. Junction temperature detecting pin ②

Using temperature characteristic of a band gap circuit and in proportion to junction temperature, pin ② DC voltage : V_2 rises at about ± 10mV / °C temperature characteristic. So, the relation between V_2 at $T_j = 25°C$ and $V_{2\chi}$ at $T_j = \chi°C$ is decided by the following expression :

$$T_j\ (\chi°C) = \frac{V_{2\chi} - V_2\ (25°C)}{10mV/°C} + 25\ (°C)$$

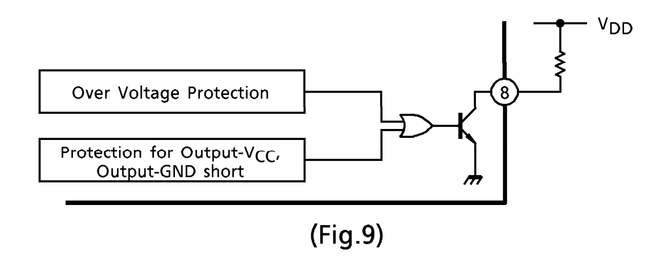
In deciding a heat sink size, a junction temperature can be easily made clear by measuring voltage at this pin while a backside temperature of IC was so far measured using a thermocouple type thermometer.



(Fig.8)

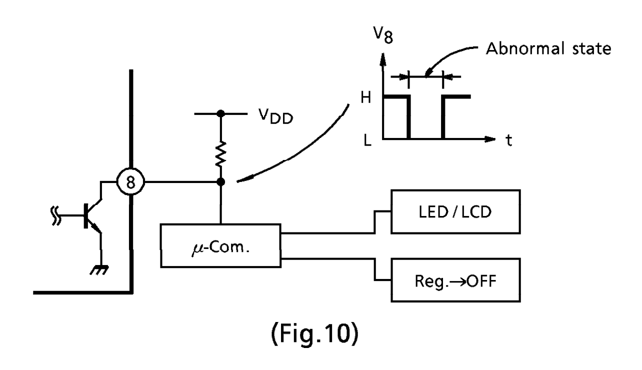
5. Output-V_{CC} short, output-GND short and over voltage detecting pin ⑧

In case of such abnormalities as output-V_{CC} short, output-GND short, overvoltage (Fig.9), it is possible to inform the abnormal state to the outside by turning a NPN transistor is turned ON.



(Fig.9)

It is possible to improve the reliability of not only power IC but also an entire equipment by (1) display by LED and LCD and (2) by turning the power supply relay off.



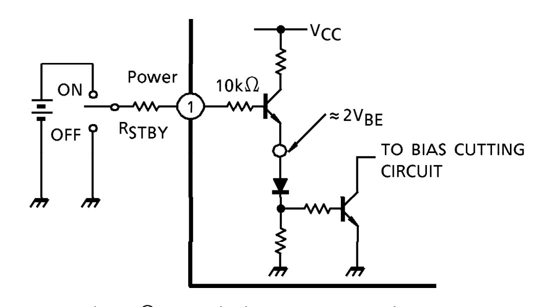
(Fig.10)

6. Stand-by SW function

By means of controlling pin ① (Stand-by terminal) to High and Low, the power supply can be set to ON and OFF.
the threshold voltage of pin ① is set at about $3V_{BE} ≒ 2.1V$ (Typ.), and the power supply current is about 1μA (Typ.) at the stand-by state.

Control Voltage of ①pin : $V_{(SB)}$

Stand-By	Power	$V_{(SB)}$ (V)
ON	OFF	0~2
OFF	ON	3~V_{CC}

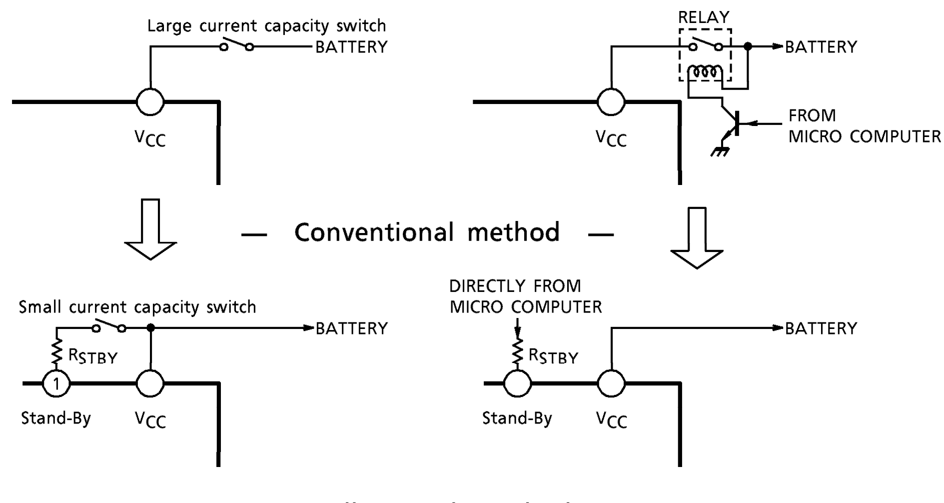


With pin ① set to high, power is turned ON.

(Fig.11)

<Caution>

Must be set the control voltage value less than V_{CC} when the stand-by terminal (Pin ①) is applied. In this case, we recommended the series connecting resistance for current limit : R_{STBY} (100kΩ~1kΩ to pin ①.)



— Standby switch method —

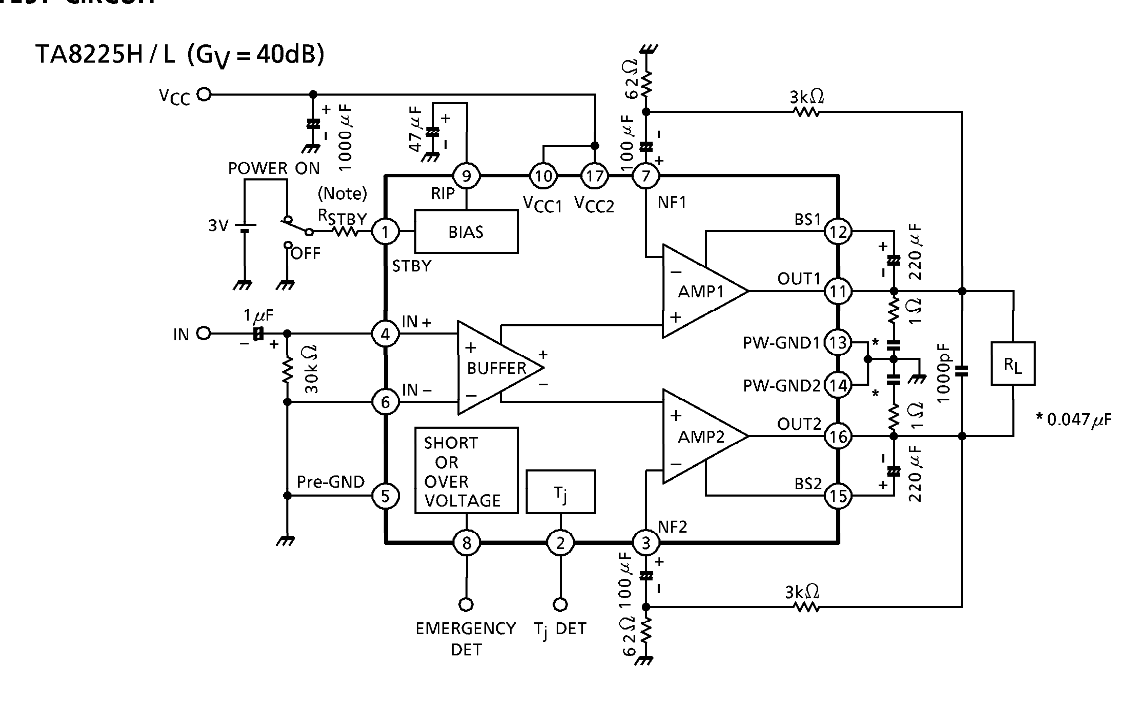
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage (0.2s)	$V_{CC\,(surge)}$	50	V
DC Supply Voltage	$V_{CC\,(DC)}$	25	V
Operating Supply Voltage	$V_{CC\,(opr)}$	18	V
Output Current (Peak)	$I_{O\,(peak)}$	9	A
Power Dissipation	P_D	50	W
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~150	°C

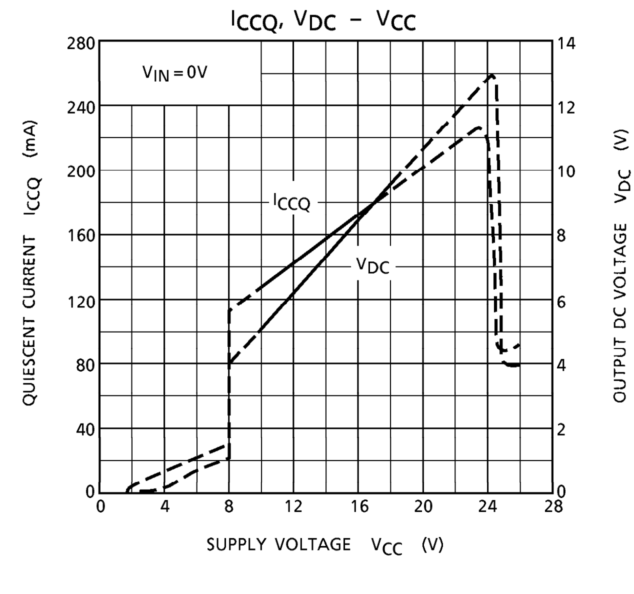
ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, V_{CC} = 13.2V, R_L = 4Ω, R_g = 600Ω, f = 1kHz, Ta = 25°C)

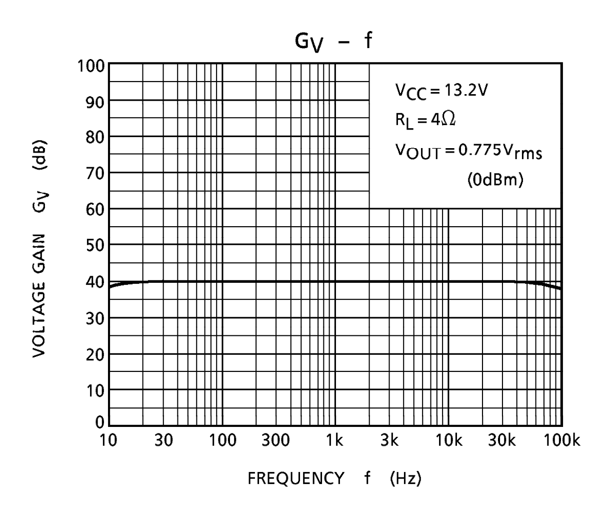
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_{CCQ}	—	V_{IN} = 0	—	150	250	mA
Output Power	P_{OUT} (1)	—	V_{CC} = 14.4V, THD = 10%, R_L = 2Ω	—	45	—	W
	P_{OUT} (2)	—	THD = 10%, R_L = 2Ω	33	40	—	W
	P_{OUT} (3)	—	THD = 10%	20	24	—	W
	P_{OUT} (4)	—	THD = 1%, f = 50Hz~20kHz	—	18	—	W
Total Harmonic Distortion	THD	—	P_{OUT} = 4W	—	0.015	0.07	%
Voltage Gain	G_V	—	V_{IN} = 10mV$_{rms}$	38.5	40	41.5	dB
Output Noise Voltage	V_{NO} (1)	—	R_g = 0, DIN45405 Noise filter	—	0.26	—	mV$_{rms}$
	V_{NO} (2)	—	R_g = 0, BW = 20Hz~20kHz	—	0.23	0.5	mV$_{rms}$
Ripple Rejection Ratio	R.R.	—	f = 100Hz, V_{ripple} = 0.775V$_{rms}$ (0dBm)	50	60	—	dB
Output Offset Voltage	V_{offset}	—	V_{IN} = 0	– 100	0	100	mV
Current at Stand-By State	I_{SB}	—	—	—	1	30	μA

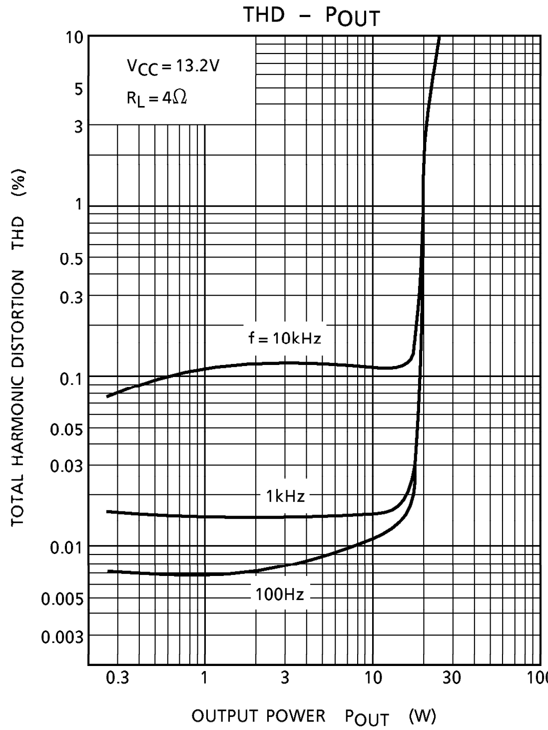
TEST CIRCUIT

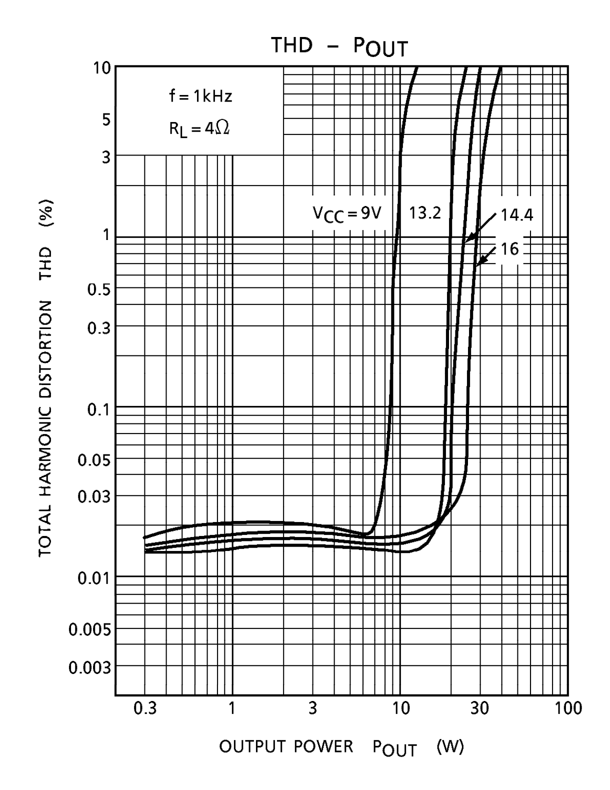


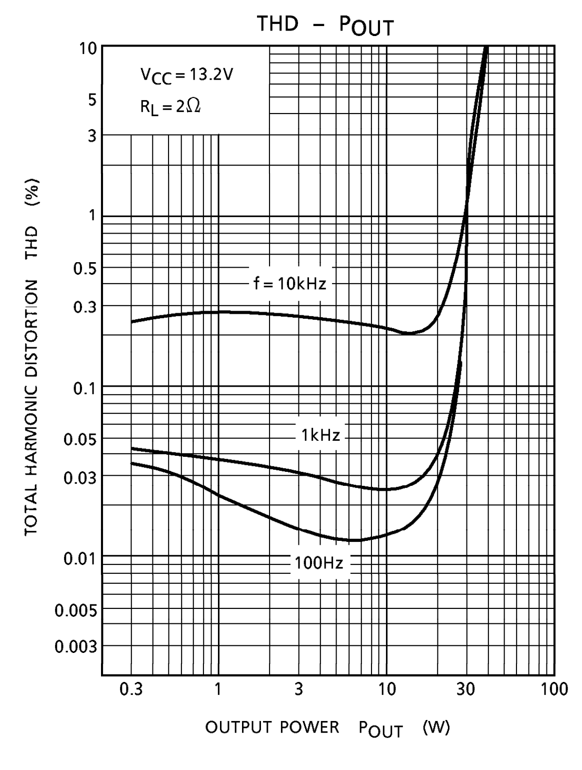
(Note) The purpose of R_{STBY} is current limiting resistance.

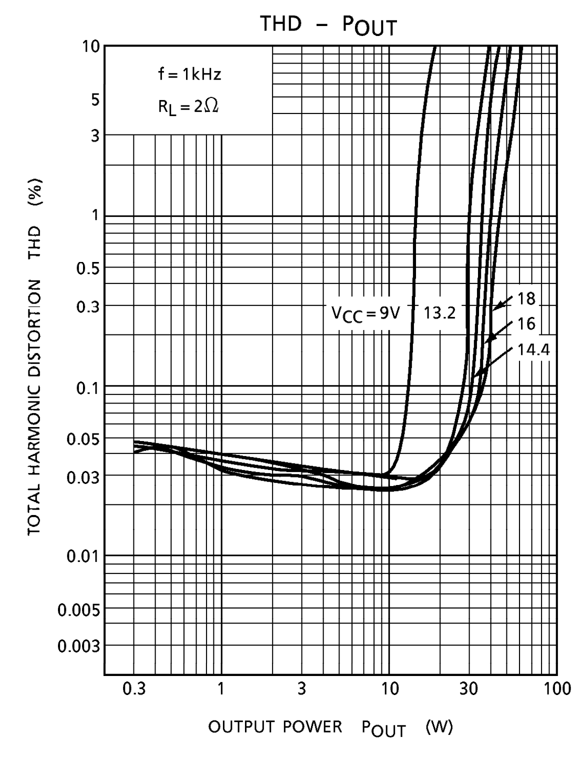

ICCQ, VDC – VCC
VIN = 0V
ICCQ
VDC
QUIESCENT CURRENT ICCQ (mA)
OUTPUT DC VOLTAGE VDC (V)
SUPPLY VOLTAGE VCC (V)
0 4 8 12 16 20 24 28
0 40 80 120 160 200 240 280
0 2 4 6 8 10 12 14

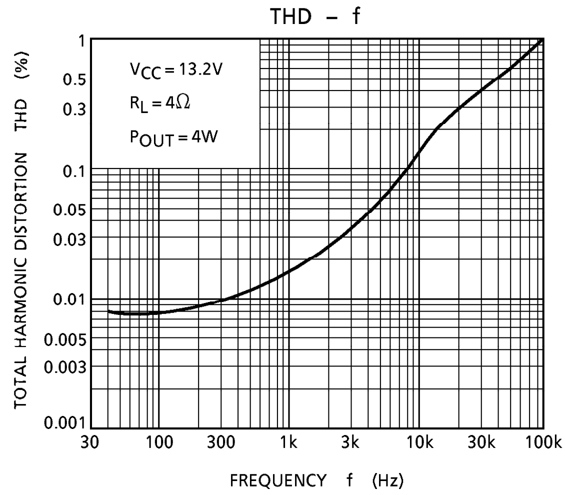

GV – f
VCC = 13.2V
RL = 4Ω
VOUT = 0.775Vrms
(0dBm)
VOLTAGE GAIN GV (dB)
FREQUENCY f (Hz)
10 30 100 300 1k 3k 10k 30k 100k
0 10 20 30 40 50 60 70 80 90 100

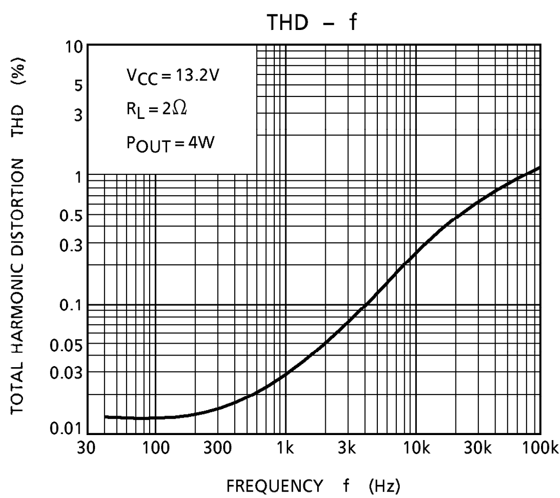

THD – POUT
VCC = 13.2V
RL = 4Ω
f = 10kHz
1kHz
100Hz
TOTAL HARMONIC DISTORTION THD (%)
OUTPUT POWER POUT (W)
0.3 1 3 10 30 100
0.003 0.005 0.01 0.03 0.05 0.1 0.3 0.5 1 3 5 10

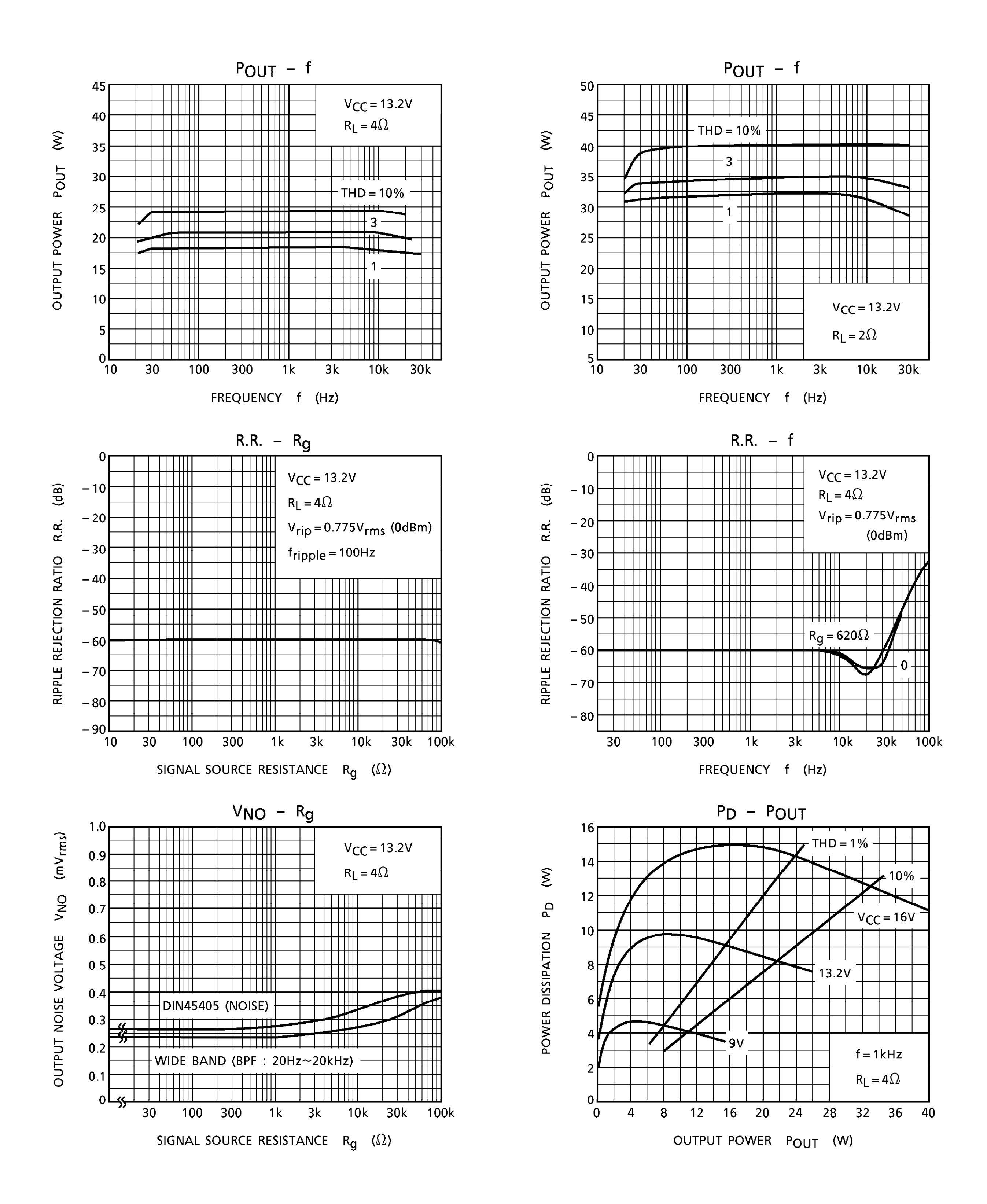

THD – POUT
f = 1kHz
RL = 4Ω
VCC = 9V
13.2
14.4
16
TOTAL HARMONIC DISTORTION THD (%)
OUTPUT POWER POUT (W)
0.3 1 3 10 30 100
0.003 0.005 0.01 0.03 0.05 0.1 0.3 0.5 1 3 5 10


THD – POUT
VCC = 13.2V
RL = 2Ω
f = 10kHz
1kHz
100Hz
TOTAL HARMONIC DISTORTION THD (%)
OUTPUT POWER POUT (W)

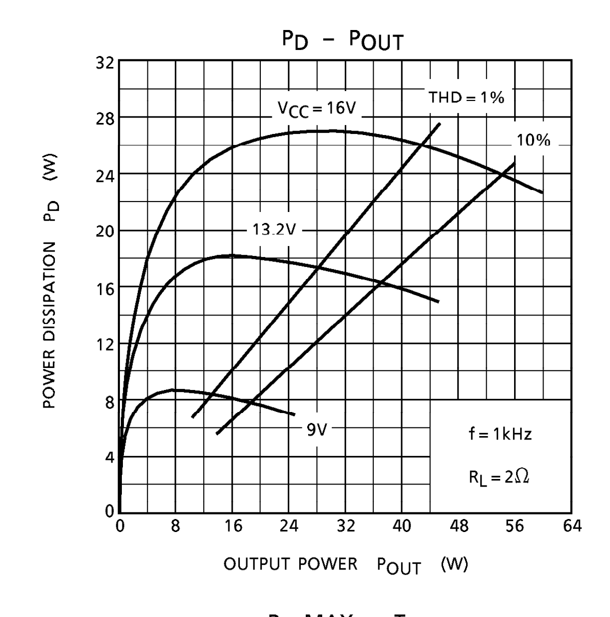

THD – POUT
f = 1kHz
RL = 2Ω
VCC = 9V
13.2
18
16
14.4
TOTAL HARMONIC DISTORTION THD (%)
OUTPUT POWER POUT (W)

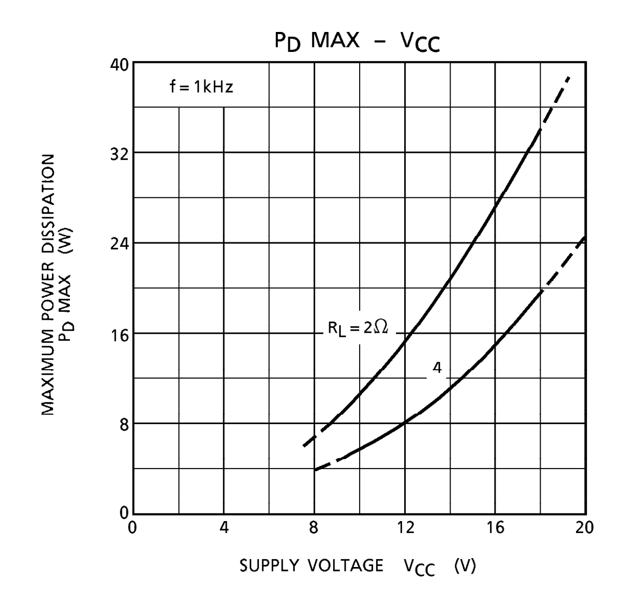

THD – f
VCC = 13.2V
RL = 4Ω
POUT = 4W
TOTAL HARMONIC DISTORTION THD (%)
FREQUENCY f (Hz)

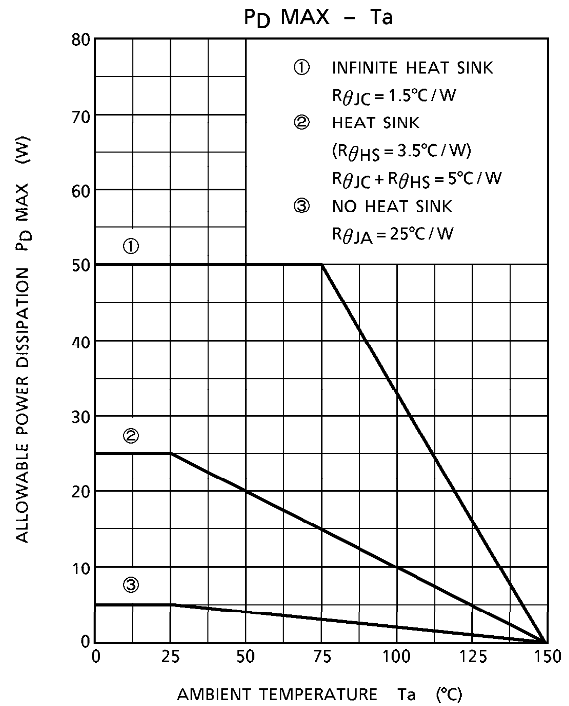

THD – f
VCC = 13.2V
RL = 2Ω
POUT = 4W
TOTAL HARMONIC DISTORTION THD (%)
FREQUENCY f (Hz)



POUT – f
VCC = 13.2V
RL = 4Ω
THD = 10%
3
1
OUTPUT POWER POUT (W)
FREQUENCY f (Hz)
POUT – f
THD = 10%
3
1
VCC = 13.2V
RL = 2Ω
OUTPUT POWER POUT (W)
FREQUENCY f (Hz)
R.R. – Rg
VCC = 13.2V
RL = 4Ω
Vrip = 0.775Vrms (0dBm)
fripple = 100Hz
RIPPLE REJECTION RATIO R.R. (dB)
SIGNAL SOURCE RESISTANCE Rg (Ω)
R.R. – f
VCC = 13.2V
RL = 4Ω
Vrip = 0.775Vrms
(0dBm)
Rg = 620Ω
0
RIPPLE REJECTION RATIO R.R. (dB)
FREQUENCY f (Hz)
VNO – Rg
VCC = 13.2V
RL = 4Ω
DIN45405 (NOISE)
WIDE BAND (BPF : 20Hz~20kHz)
OUTPUT NOISE VOLTAGE VNO (mVrms)
SIGNAL SOURCE RESISTANCE Rg (Ω)
PD – POUT
THD = 1%
10%
VCC = 16V
13.2V
9V
f = 1kHz
RL = 4Ω
POWER DISSIPATION PD (W)
OUTPUT POWER POUT (W)


P_D – P_{OUT}
V_{CC} = 16V
THD = 1%
10%
13.2V
9V
f = 1kHz
R_L = 2Ω
POWER DISSIPATION P_D (W)
OUTPUT POWER P_{OUT} (W)
0 8 16 24 32 40 48 56 64
0 4 8 12 16 20 24 28 32

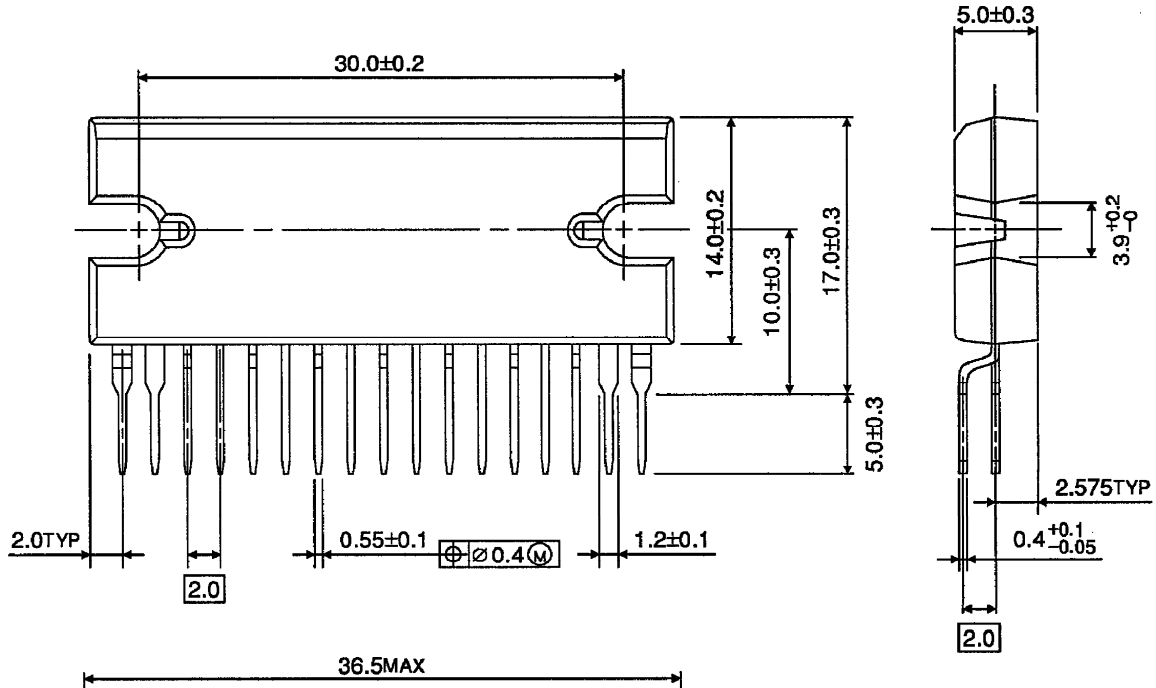

P_D MAX – V_{CC}
f = 1kHz
R_L = 2Ω
4
MAXIMUM POWER DISSIPATION P_D MAX (W)
SUPPLY VOLTAGE V_{CC} (V)
0 4 8 12 16 20
0 8 16 24 32 40

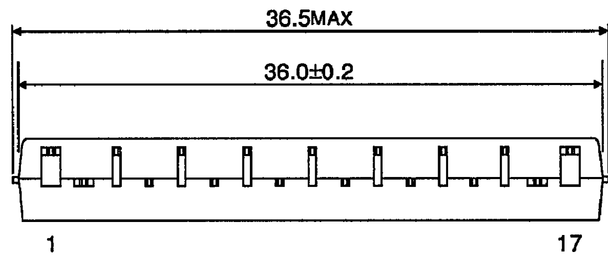

P_D MAX – Ta
① INFINITE HEAT SINK
$R_{\theta JC}$ = 1.5°C / W
② HEAT SINK
($R_{\theta HS}$ = 3.5°C / W)
$R_{\theta JC}$ + $R_{\theta HS}$ = 5°C / W
③ NO HEAT SINK
$R_{\theta JA}$ = 25°C / W
①
②
③
ALLOWABLE POWER DISSIPATION P_D MAX (W)
AMBIENT TEMPERATURE Ta (°C)
0 25 50 75 100 125 150
0 10 20 30 40 50 60 70 80

OUTLINE DRAWING

HZIP17-P-2.00

Unit : mm





Weight : 9.8g (Typ.)

OUTLINE DRAWING
HSIP17-P-2.00

Unit : mm

30.0±0.2
5.0±0.3
14.0±0.2
17.0±0.3
10.0±0.3
5.0±0.3
$3.9^{+0.2}_{-0}$
2.575TYP
$0.4^{+0.1}_{-0.05}$
2.0TYP
2.0
0.55±0.1
⌀0.2 M
1.2±0.1
36.5MAX
36.0±0.2
1
17

Weight : 9.8g (Typ.)